UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,401	09/29/2003	Kuo-Chien Wu	10587-US-PA	2400

31561 7590 03/01/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
DANG, PHUC T	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,401	WU ET AL.	
	Examiner	Art Unit	
	PHUC T DANG	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-10,12-14 and 16-18* is/are rejected.

7)☒ Claim(s) *2,7,11 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on September 29, 2003 is acceptable.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections-35 USC § 112

4. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

In claim 1, step of "planarizing the dielectric layer the cap layer of the gate structures and the bit line contact is exposed" are indefinite since it is unclear to point out the subject matter which Applicants regard as the invention?

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 4-6 and 8 are rejected under 35 U.S.C. 102 (b) as being anticipated by Lee (U.S. Patent No. 6,228,700 B1).

Lee discloses a method of forming bit lines and bit line contacts of a memory device, comprising the steps of:

providing a substrate (200, Fig. 3A) having a plurality of gate structures (Fig. 3B) thereon, wherein each gate structure comprises a gate dielectric layer (300, Fig. 3B), a gate conductive layer (302, Fig. 3B) and a cap layer (304, Fig. 3B), and wherein a spacer (308, Fig. 3B0 is formed on each sidewall of the gate structure;

forming a conductive layer over the substrate to cover the gate structures;

planarizing the conductive layer until the cap layer of the gate structures is exposed;

removing a portion of the conductive layer but retaining the conductive layer between neighboring gate structures to form a bit line contact (314, Fig. 3C);

forming a dielectric layer (320, Fig. 3D) over the substrate to cover the gate structures and the bit line contact (314, Fig. 3D);

planarizing the dielectric layer (320, Fig. 3E) until the cap layer (304, Fig. 3E) of the gate structures and the bit line contact (304, Fig. 3E) is exposed; and

forming a bit line (324, Fig. 3E) over the dielectric layer (320, Fig. 3E), wherein the bit line (324, Fig. 3E) and the bit line contact (314, Fig. 3E) are electrically connected.

Regarding claim 4, Lee discloses the step of forming the bit line over the dielectric layer comprises forming a first dielectric layer over the dielectric layer; forming a trench (322, Fig. 3D) in the first dielectric layer such that the trench exposes the bit line contact (314, Fig. 3D); and depositing conductive material into the trench to form the bit line (324, Fig. 3E).

Regarding claims 5-6, Lee discloses the step of planarizing the conductive layer and the dielectric layer comprise performing a chemical mechanical polishing operation [col. 5, lines 5-8].

Regarding claim 8, Lee discloses the material constituting the bit line contact comprises doped polysilicon [col. 5, lines 1-8].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Park et al. (U.S. Patent No. 6,071,799).

Lee discloses all the features of the claimed invention as discussed above, but does not disclose a step of forming a barrier layer over the substrate and the gate structures; and removing the barrier layer between two neighboring gate structures to expose the substrate before forming the conductive layer over the substrate.

Park et al., however, disclose a step of forming a barrier layer over the substrate and the gate structures; and removing the barrier layer between two neighboring gate structures to expose the substrate before forming the conductive layer over the substrate [Fig. 4].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Park et al. to Lee discussed above such that a step of forming a barrier layer over the substrate and the gate structures; and removing the barrier layer between two neighboring gate structures to expose the substrate before forming the conductive layer over the substrate for a purpose of improving a process of forming bit lines and bit line contacts of a memory device.

7. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Nam et al. (U.S. Patent No. 5,728,627).

Lee discloses all the features of the claimed invention as discussed above, but does not disclose the material constituting the bit line contact comprises tungsten.

Nam et al., however, discloses the material constituting the bit line contact comprises tungsten [col. 2, lines 24-27].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Nam et al. to Lee discussed above such that the

material constituting the bit line contact comprises tungsten for a purpose of improving a process of forming bit lines and bit line contacts of a memory device.

8. Claims 10, 13-14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Nam et al. (U.S. Patent No. 5,728,627).

Regarding claims 10 and 16, Lee discloses all the features of the claimed invention as discussed above, but does not disclose a process comprises providing a substrate comprising a memory cell region and a peripheral circuit region and forming a bit line over the dielectric layer so that a contact is also formed within the dielectric layer in the peripheral circuit region, wherein the bit line is electrically connected to both the bit line contact and the contact and a step of forming an opening in the dielectric layer at the bottom of the trench within the peripheral circuit region, wherein the opening exposes the substrate.

A process comprises providing a substrate comprising a memory cell region and a peripheral circuit region and forming a bit line over the dielectric layer so that a contact is also formed within the dielectric layer in the peripheral circuit region, wherein the bit line is electrically connected to both the bit line contact and the contact and a step of forming an opening in the dielectric layer at the bottom of the trench within the peripheral circuit region, wherein the opening exposes the substrate is considered to be obvious in variation design, since each memory device is used to have the memory cell region and the peripheral circuit region built in the active area.

Thus, it would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply a process comprises providing a substrate comprising a memory

cell region and a peripheral circuit region and forming a bit line over the dielectric layer so that a contact is also formed within the dielectric layer in the peripheral circuit region, wherein the bit line is electrically connected to both the bit line contact and the contact and a step of forming an opening in the dielectric layer at the bottom of the trench within the peripheral circuit region, wherein the opening exposes the substrate, as suggested in Lee reference in Fig. 3E, the active region 204 for a purpose of improving a process of forming bit lines and bit line contacts of a memory device.

Regarding claims 13-14, Lee discloses the step of planarizing the conductive layer and the dielectric layer comprise performing a chemical mechanical polishing operation [col. 5, lines 5-8].

Regarding claim 16, Lee discloses all the features of the claimed invention as discussed above, but does not disclose a step of forming an opening in the dielectric layer at the bottom of the trench within the peripheral circuit region, wherein the opening exposes the substrate.

Regarding claim 17, Lee discloses the material constituting the bit line contact comprises doped polysilicon [col. 5, lines 1-8].

Allowable Subject Matter

9. Claims 2, 7, 11 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-872-9306 for After Final communications.

12. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

PD

Phuc T. Dang

Primary Examiner

Art Unit 2818

February 18, 2004